

MAR 15 2011

cadence™

Cadence Design Systems, Inc.
2655 Seely Avenue
San Jose, CA 95134
Tel: 408-428-5340

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent: 7093220

Issue Date: 8/15/2006

Title: METHOD FOR GENERATING CONSTRAINED COMPONENT PLACEMENT
FOR INTEGRATED CIRCUITS AND PACKAGES

Our Ref: 04PA064US01

Commissioner for Patents
United States Patent and Trademark Office
Washington DC 20231

LARGE ENTITY ASSERTION

Please note that the United States patent mentioned above qualifies as a large entity.
Please immediately update the patent record to reflect large entity status for this case.

Thank you for your attention to this matter.

Regards,

Nancy I. Sya
Nancy I. Sya
Reg. No. 52266